AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) An information communication system, comprising:

a plurality of information communication devices, wherein each of the plurality of information communication devices is responsive to a respective information communication clock signal, and wherein ~~each~~ the information communication clock ~~signal~~ signals are ~~of each of the plurality of information communication devices is~~ associated with a common reference clock signal; and

a phase controller comprising ~~controller,~~

~~wherein the phase controller is responsive to the common reference clock signal,~~ ~~and~~

a phase locked loop configured to generate an output signal based on the common reference clock signal;

a signal division controller configured to generate a divider reset signal based on the common reference clock signal, the output signal, and a select signal; and

a divider configured to generate one of the information communication clock signals by performing frequency division of the output signal based on the divider reset signal, wherein the divider reset signal controls a start time of the frequency division.

~~wherein the phase controller alters a phase of each information communication clock signal of each of the plurality of information communication devices by a predetermined amount to at least double a combined amplitude of individual waveforms of output current events of the plurality of information communication devices.~~

2. (Cancelled)

3. (Currently Amended) The information communication system of ~~claim 2~~ claim 1, wherein the phase controller ~~alters a~~ is configured to stagger each phase of the ~~common reference clock signal for each of the plurality of information communication devices by the predetermined amount to alter the phase of each~~ information communication clock ~~signal of each of the plurality of information communication devices by the~~ signals by a predetermined amount.

4. (Currently Amended) The information communication system of claim 1, further comprising ~~comprising:~~ a reference clock signal generator ~~for generating~~ configured to generate the common reference clock signal.

5. (Currently Amended) The information communication system of claim 3 ~~claim 1~~, wherein the ~~phase controller alters the phase of each information communication clock signal of each of the plurality of information communication devices by~~ predetermined amount is a multiple of 90 degrees.

6. (Currently Amended) The information communication system of claim 1,

wherein ~~the phase~~ phases of ~~at least two of~~ a number of the information communication clock signals are substantially identical,

wherein the number is at least two, and

wherein ~~a~~ the number ~~of information communication clock signals with substantially identical phase~~ is less than a total number of the information communication clock signals ~~of the information communication system~~.

7-11. (Cancelled)

12. (Currently Amended) The information communication system of claim 1, wherein ~~the information communication system~~ at least one of the plurality of information communication devices comprises an Ethernet transceiver.

13. (Currently Amended) The information communication system of claim 12, wherein the Ethernet transceiver is compliant with ~~I.E.E.E. 802.3ab~~ IEEE 802.3ab.

14-108. (Cancelled)

109. (New) The information communication system of claim 1, wherein the select signal is binary, wherein the divider is configured to divide a frequency of the output signal by an integer, and wherein the integer is equal to a number of possible values of the select signal.

110. (New) The information communication system of claim 109, wherein the number of possible values of the select signal is equal to a total number of the information communication devices.

111. (New) The information communication system of claim 1, wherein the signal division controller is configured to generate the divider reset signal further based on a system reset signal.

112. (New) The information communication system of claim 1, further comprising:

a plurality of dividers,

wherein the plurality of dividers includes the divider, and

wherein each of the plurality of dividers generates a corresponding one of the information communication clock signals by performing frequency division of the output signal.

113. (New) The information communication system of claim 112, further comprising:

a plurality of signal division controllers,

wherein the plurality of signal division controllers includes the signal division controller,

wherein each of the plurality of signal division controllers generates a divider reset signal, and

wherein each of the plurality of dividers generates the corresponding one of the information communication clock signals based on a corresponding divider reset signal.

114. (New) A multi-port network device compliant with IEEE 802.3ab, comprising the information communication system of claim 1.

115. (New) A method, comprising:

using a phase locked loop, generating an output signal based on a common reference clock signal;

generating a divider reset signal based on the common reference clock signal, the output signal, and a select signal;

generating a communication clock signal by performing frequency division of the output signal based on the divider reset signal, wherein the divider reset signal controls a start time of the frequency division; and

controlling a plurality of communication devices based on a plurality of communication clock signals, respectively,

wherein the plurality of communication clock signals includes the communication clock signal.

116. (New) The method of claim 115, further comprising:

generating a plurality of divider reset signals based on a plurality of select signals, respectively, wherein the plurality of divider reset signals includes the divider reset signal, wherein the plurality of select signals includes the select signal, and wherein the plurality of divider reset signals are generated based also on the common reference clock signal and the output signal; and

generating the plurality of communication clock signals by performing frequency division of the output signal based on the plurality of divider reset signals, respectively.

117. (New) The method of claim 116, wherein each of the plurality of select signals is a different value.

118. (New) The method of claim 115, wherein the select signal is binary, wherein the frequency division divides a frequency of the output signal by an integer, and wherein the integer is equal to a number of possible values of the select signal.

119. (New) The method of claim 118, wherein the number of possible values of the select signal is equal to a total number of the plurality of communication devices.

120. (New) The method of claim 115, wherein the divider reset signal is further based on a system reset signal.

121. (New) The method of claim 115, further comprising staggering each phase of the plurality of communication clock signals by a predetermined amount.

122. (New) The method of claim 121, wherein the predetermined amount is a multiple of 90 degrees.

123. (New) The method of claim 115, wherein phases of a number of the plurality of communication clock signals are substantially identical, wherein the number is at least two, and wherein the number is less than a total number of the plurality of communication clock signals.

124. (New) The method of claim 115, further comprising generating the common reference clock signal.

125. (New) The method of claim 115, wherein the method is compliant with IEEE 802.3ab.